IN THE CLAIMS:

Please cancel claims 1-4, 7-12, and 15-19 in their entirety without prejudice nor disclaimer of the subject matter set forth therein

1.-4. (Canceled)

5. (Currently Amended) ~~The method of claim 1, further~~ A method of laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core ring with a first power line and a first ground line, the first power line and the first ground line being mutually adjacent, the core ring supplying power to circuits surrounded by the core ring, the method comprising:

routing a plurality of the metal interconnecting lines across the core ring, for use as input-output (I/O) signal lines;

identifying a part of the core ring crossed by comparatively few of the I/O signal lines; ~~and~~

laying out ~~placing said~~ at least one metal-oxide-semiconductor (MOS) ~~MOS~~ capacitor unit below said part of the core ring, the MOS capacitor unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, at least part of the insulated gate electrode being disposed above part of the active area;

laying out first contacts connecting the active area to one of the first power line and the first ground line, and;

laying out second contacts connecting the insulated gate electrode to another one of the first power line and the first ground line.

6. (Currently Amended) ~~The method of claim 1, further~~ A method of laying out

an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core ring with a first power line and a first ground line, the first power line and the first ground line being mutually adjacent, the core ring supplying power to circuits surrounded by the core ring, the method comprising:

calculating an antenna ratio of the first power line; ~~and~~

calculating an antenna ratio of the first ground line;

laying out at least one metal-oxide-semiconductor (MOS) capacitor unit below the core ring, the MOS capacitor unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, at least part of the insulated gate electrode being disposed above part of the active area;

laying out first contacts connecting the active area to one of the first power line and the first ground line, and;

laying out second contacts connecting the insulated gate electrode to another one of the first power line and the first ground line;

wherein laying out said second contacts includes

connecting the insulated gate electrode to the first power line if the antenna ratio of the first power line is greater than the antenna ratio of the first ground line; and

connecting the insulated gate electrode to the first ground line if the antenna ratio of the first ground line is greater than the antenna ratio of the first power line.

7.-12. (Canceled)

13. (Currently Amended ~~The method of claim 9, further~~ A method of laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core

ring with a first power line and a first ground line and an input-output (I/O) ring with a second power line and a second ground line, the first power line and the first ground line being mutually adjacent, the second power line and the second ground line being mutually adjacent, the I/O ring and the core ring being mutually adjacent, the I/O ring surrounding the core ring, the core ring supplying power to circuits surrounded by the core ring, the I/O ring supplying power to I/O circuits disposed outside the core ring, the method comprising:

routing a plurality of the metal interconnecting lines from the circuits surrounded by the core ring to the I/O circuits, for use as I/O signal lines;

identifying a part of the core ring crossed by comparatively few of the I/O signal lines; ~~and~~

laying out a ~~placing said~~ plurality of MOS units ~~under~~ below said part of the core ring and below the I/O ring, each MOS unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, the active area underlying the first power line, the first ground line, the second power line, and the second ground line, the insulated gate electrode paralleling the active area and having a plurality of branches overlying the active area; and

laying out contacts connecting the MOS units to the core ring and the I/O ring, the contacts causing at least a first one of the MOS units to function as a MOS capacitor connected to the core ring, and at least a second one of the MOS units to function as a protection transistor connected to both the core ring and the I/O ring.

14. (Currently Amended) ~~The method of claim 9, further~~ A method of laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core ring with a first power line and a first ground line and an input-output (I/O) ring with a

second power line and a second ground line, the first power line and the first ground line being mutually adjacent, the second power line and the second ground line being mutually adjacent, the I/O ring and the core ring being mutually adjacent, the I/O ring surrounding the core ring, the core ring supplying power to circuits surrounded by the core ring, the I/O ring supplying power to I/O circuits disposed outside the core ring, the method comprising:

laying out a plurality of MOS units below the core ring and the I/O ring, each MOS unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, the active area underlying the first power line, the first ground line, the second power line, and the second ground line, the insulated gate electrode paralleling the active area and having a plurality of branches overlying the active area;

calculating an antenna ratio of the first power line; ~~and~~

calculating an antenna ratio of the first ground line; and

laying out contacts connecting the MOS units to the core ring and the I/O ring, the contacts causing at least a first one of the MOS units to function as a MOS capacitor connected to the core ring, and at least a second one of the MOS units to function as a protection transistor connected to both the core ring and the I/O ring;

wherein

if the antenna ratio of the first power line is greater than the antenna ratio of the first ground line, the contacts connect the insulated gate electrode of the first MOS unit to the first power line and connect the active area of the first one of the MOS units to the first ground line; and

if the antenna ratio of the first ground line is greater than the antenna ratio of the first power line, the contacts connect the insulated gate electrode of the first one of the

MOS units to the first ground line and connect the active area of the first MOS unit to the first power line.

15.-19. (Canceled)